The following Listing of Claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

1-13. (Canceled)

14. (Previously Presented) In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode, a method for processing a semiconductor wafer through plasma etching operations, comprising:

striking a plasma in a plasma region of the chamber; and

generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode, the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface which is located over the wafer surface of the semiconductor wafer,

wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath

surface having a second plasma sheath surface area that is proximate to the second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area.

15. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

causing the second plasma sheath surface having the second plasma sheath surface area to shift into the electrode openings of the second surface of the top electrode, the electrode openings being at least 0.5 mm or greater in diameter and the gas feed holes having a diameter of about 0.1 mm.

17. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the second surface and the wafer surface.

19. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at between about 0.5 mm and about 5 mm.

21. (Previously Presented) The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath surface area is greater than the first plasma sheath surface area.

22-32. (Canceled).

33. (Previously Presented) A method of processing a semiconductor wafer, comprising:

providing a processing chamber, the processing chamber being in an operational state and including a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources;

striking a plasma within a plasma region of the processing chamber; and

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode,

wherein the plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

34. (Previously Presented) The method of processing a semiconductor wafer as recited in claim 33, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of the second surface of the plasma sheath.

35. (Previously Presented) The method of processing a semiconductor wafer as recited in claim 33, further comprising increasing a bias voltage over the surface of the semiconductor wafer while slightly decreasing the bias voltage over a surface of the top electrode and without increasing a plasma density.

36. (Previously Presented) The method of processing a semiconductor wafer as recited in claim 33, wherein the top electrode has a center region, a first surface and a second surface, the first surface of the top electrode having an inlet that is configured to receive

processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the second surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface of the top electrode which is located over the surface of the semiconductor wafer.

37. (Previously Presented) A method for high aspect ratio semiconductor etching, comprising:

providing a plasma etch processing chamber, the plasma etch processing chamber including a top electrode, a wafer support chuck, and a pair of RF power supplies, and the plasma etch processing chamber being configured in an operational state;

striking a plasma in a plasma region of the plasma etch processing chamber, the plasma region being defined between an electrode surface of the top electrode and a wafer surface of a wafer positioned on the wafer support chuck;

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode, the first surface of the plasma sheath being proximate to the top electrode; and

increasing a bias voltage over the wafer surface while decreasing the bias voltage over the electrode surface of the top electrode and without increasing a plasma density.

38. (Previously Presented) The method for high aspect ratio semiconductor etching of claim 37, further comprising increasing an ion bombardment energy on the wafer surface.

39. (Previously Presented) The method for high aspect ratio semiconductor etching of claim 37, wherein the top electrode has a center region, a first surface and the electrode surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the electrode surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the electrode surface of the top electrode which is located over the wafer surface.

40. (Previously Presented) The method for high aspect ratio semiconductor etching of claim 37, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of a second surface of the plasma sheath, the second surface of the plasma sheath being defined proximate to the wafer surface.